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GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	6

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,950	THURSTON, ANDREW J.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/5/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The legal phraseology "means" used in the abstract should be removed.

Claim Objections

2. Claim 4 is objected to because of the following informalities: On page 40, line 2 of claim 4;

"period" is missing at the end of the sentence. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to

particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 9, do, d1, d2 and q0, q1 are not defined. What is relationship between x and X?

5. Claim 38 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to

particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 38, do, d1, d2 and q0, q1 are not defined. What is relationship between x and X?

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for

the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 5, 9, 10, 11, 12, 25, 30, 31, 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Shen et al. (US 6,199,188 B1).

Shen et al. anticipate claim 1.

Shen et al. teach a method of decoding an error-correction code in a data signal, comprising the steps of: receiving the data signal at a decoding unit; computing a plurality of syndromes associated with the data signal using the decoding unit; extracting an error polynomial from the data signal based on no more than six equations having no more than two branch decisions; and locating errors within the data signal using the error polynomial (figure 1, 2, col. 4, lines 36-48, col. 7, line 8 - col. 8, line 3, Shen et al.).

- Shen et al. anticipate claim 5.

Shen et al. teach the method wherein said computing, extracting, and locating steps use a Bose-chaudhuri-Hocquenghem (BCH) code (col. 1, lines 49-58, Shen et al.).

- Shen et al. anticipate claim 9.

Shen et al. teach the method wherein the generating step generates the error polynomial based on the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(x) = 1 + S_1X$,

(4) if ($d_1 = 0$) then $\sigma^2(x) = \sigma^1(x)$

else if ($d_0 = 0$) then $\sigma^2(x) = q_0\sigma^1(x) + d_1X^3$

else $\sigma^2(x) = q_0\sigma^1(x) + d_1X^2$,

(5) $d_2 = S_5\sigma 0 + S_4\sigma 1 + S_3\sigma 2 + S_2\sigma 3$, and

(6) if ($d_2 = 0$) then $\sigma^3(x) = \sigma^2(x)$

else $\sigma^3(x) = q_1\sigma^1(x) + d_1X^3$,

where S_i are the syndromes, σ^i are minimum-degree polynomials, σ_1 are four coefficients for $\sigma^2(x)$, q_0 is equal to d_0 unless d_0 is zero, when q_0 is 1, and q_1 is equal to d_1 unless d_1 is zero, when $q_1 = q_0$ (col. 7, line 7 – col. 8, line 3, Shen et al.).

- Shen et al. anticipate claim 10.

Shen et al. teach the method wherein said generating step includes the step of calculating correction terms using four Galois field multiply accumulators (col. 21, lines 19-21, col. 21, line 52 - col. 22, line 8, Shen et al.).

- Shen et al. anticipate claim 11.

Shen et al. teach the method wherein said locating step locates the errors by determining roots of the error polynomial, which correspond to error locations (col. 1, lines 55-57, Shen et al.).

- Shen et al. anticipate claim 12.

Shen et al. teach the method wherein the locating step uses Chien's algorithm to search for the error location numbers (col. 2, lines 1-15, Shen et al.).

- Shen et al. anticipate claim 25.

Shen et al. teach a circuit for generating an error polynomial of a Bose-chaudhuri-Hocquenghem (BCH) code, comprising: a plurality of syndrome inputs (col. 1, lines 49-52, Shen et al.), a plurality of Galois field multiply accumulators (figure 4, col. 12, lines 30-33, Shen et al.); and means for using said Galois field multiply accumulators to generate an error polynomial based on values provided at said syndrome inputs (col. 1, lines 53-55, Shen et al.), by executing no more than six equations with two branch decisions (col. 7, line 8 – col. 8, line 3, Shen et al.).

- Shen et al. anticipate claim 30.

Shen et al. teach the circuit wherein said using means uses the Galois field multiply accumulators to calculate a plurality of minimum-degree polynomials associated with the BCH code (figure 4, col. 1, lines 49-51, col. 7, lines 8-10, col. 12, lines 30-33, Shen et al.).

- Shen et al. anticipate claim 31.

Shen et al. teach the circuit wherein said using means uses the Galois field multiply accumulators to calculate a plurality of coefficients of at least one of the minimum-degree polynomials (figure 4, col. 3, lines 9-40, col. 12, lines 30-33, Shen et al.).

- Shen et al. anticipate claim 32.

Shen et al. teach the circuit wherein the BCH code is a triple-error correcting code; and said using means uses the Galois field multiply accumulators to calculate at least three minimum-degree polynomials (figure 4, col. 1, lines 49-51, col. 7, lines 8-10, col. 12, lines 30-33, Shen et al.).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 2-4, 6, 13, 14, 18, 24, 26, 38, 39, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) as applied to claim 1 above, and further in view of Oh et al. (US 5,583,499).

As per claim 2, Shen et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Shen et al. do not explicitly teach the specific use of the method, wherein said extracting step extracts the error polynomial in no more than 12 clock cycles.

Oh et al. in an analogous art teach that for a t-error correcting Reed-Solomon coder 6t multipliers are needed in calculating the error locator polynomial using the Berlekamp-Massey algorithm, wherein t represents the error correcting capability of the code. The syndrome values are inputted every 2-symbol clock cycles to be used in calculating the error locator polynomial. In other words, it takes two clock cycles in carrying out each iteration (col. 2, lines 19-25, Oh et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shen et al.'s patent with the teachings of Oh et al. by including an additional step of using the method, wherein the extracting step extracts the error polynomial in no more than 12 clock cycles. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method, wherein the extracting step extracts the error polynomial in no more than 12 clock cycles would provide the opportunity to reduce the time required to determine the locations of the errors.

- As per claim 3, Shen et al. and Oh et al. teach the additional limitations.

Oh et al. teach the method, wherein said extracting step includes the step of controlling a plurality of Galois field multiply accumulators using a state machine (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

- As per claim 4, Shen et al. and Oh et al. teach the additional limitations.

Shen et al. teach the method, wherein each of the plurality of Galois field multiply accumulators represents a different power of the error polynomial (figure 4, col. 12, lines 30-33, Shen et al.).

- As per claim 6, Shen et al. and Oh et al. teach the additional limitations.

Oh et al. teach the method wherein the computing steps computes 2t syndromes, where t is a number of correctable errors which the error-correcting code can correct (col. 3, lines 28-32, Oh et al.).

- As per claim 13, Shen et al. and Oh et al. teach the additional limitations.

Shen et al. teach a method of determining an error polynomial for decoding a Bose-Chaudhuri-Hocquenghem (BCH) code, comprising the steps of: computing a plurality of syndromes associated with a data signal having a BCH code embedded therein (col. 1, lines 49-52, Shen et al.); feeding the syndromes to a plurality of Galois field multiply accumulators; calculating a plurality of minimum-degree

polynomials associated with the BCH code, using the Galois field multiply accumulators (col. 21, line 52 - col. 22, line 8, Shen et al.), and generating an error polynomial based on the minimum-degree polynomials (col. 1, lines 53-55, Shen et al.).

Oh et al. teach the calculating and generating steps extracting the error polynomial in no more than 12 clock cycles (col. 2, lines 19-25, Oh et al.).

- As per claim 14, Shen et al. and Oh et al. teach the additional limitations.

Shen et al. teach the method wherein said calculating step includes the step of calculating a plurality of coefficients of at least one of the minimum-degree polynomials (col. 3, lines 9-40, Shen et al.).

- As per claim 18, Shen et al. and Oh et al. teach the additional limitations.

Shen et al. teach the method wherein: the BCH code is a triple-error correcting code; and the calculating step calculates at least three minimum-degree polynomials (col. 1, lines 49-51, col. 7, lines 8-10, Shen et al.).

- As per claim 24, Shen et al. and Oh et al. teach the additional limitations.

Shen et al. teach the method wherein there are exactly four of the Galois field multiply accumulators (col. 21, lines 19-21, col. 21, line 52 - col. 22, line 8, Shen et al.).

Oh et al. teach that the calculating step includes the step of controlling inputs to the Galois field multiply accumulators using a state machine (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

- As per claim 26, Shen et al. and Oh et al. teach the additional limitations.

Oh et al. teach the circuit wherein said using means includes a state machine, which asserts control ports on the Galois field multiply accumulators to execute the equations (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

- As per claim 38, Shen et al. and Oh et al. teach the additional limitations.

Shen et al. teach a decoder circuit (figure 1, col. 4, lines 36-37, Shen et al.) comprising: a plurality of Galois field multiply accumulators (figure 4, col. 4, lines 33-35, col. 12, lines 30-33, Shen et al.); and generating an error polynomial based on the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(x) = 1 + S_1X$,

(4) if ($d_1 = 0$) then $\sigma^2(x) = \sigma^1(x)$

else if ($d_0 = 0$) then $\sigma^2(x) = q_0\sigma^1(x) + d_1X^3$

else $\sigma^2(x) = q_0\sigma^1(x) + d_1X^2$,

(5) $d_2 = S_5\sigma 0 + S_4\sigma 1 + S_3\sigma 2 + S_2\sigma 3$, and

(6) if ($d_2 = 0$) then $\sigma^3(x) = \sigma^2(x)$

else $\sigma^3(x) = q_1\sigma^1(x) + d_1X^3$,

where S_i are the syndromes, σ^i are minimum-degree polynomials, σ_i are four coefficients for $\sigma^2(x)$, q_0 is equal to d_0 unless d_0 is zero, when q_0 is 1, and q_1 is equal to d_1 unless d_1 is zero, when $q_1 = q_0$ (col. 7, line 7 – col. 8, line 3, Shen et al.).

Oh et al. teach a state machine programmed to use the Galois field multiply accumulators (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

- As per claim 39, Shen et al. and Oh et al. teach the additional limitations.

Shen et al. teach the decoder circuit wherein each of the Galois field multiply accumulators represents a different power of the error polynomial (figure 4, col. 12, lines 30-33, Shen et al.).

- As per claim 42, Shen et al. and Oh et al. teach the additional limitations.

Shen et al. teach the decoder circuit wherein: the BCH code is a triple-error correcting code (col. 1, lines 49-51, col. 7, lines 8-10, Shen et al.); and there are exactly four of said Galois field multiply accumulators (col. 21, lines 19-21, col. 21, line 52 - col. 22, line 8, Shen et al.).

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) as applied to claim 1 above, and further in view of Erhart et al. (US 5,051,999).

As per claim 7, Shen et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Shen et al. do not explicitly teach the specific use of the method wherein the computing step uses a linear feedback register to compute the syndromes.

Erhart et al. in an analogous art teach that each shift of the linear feedback register calculates a subsequent syndrome (col. 3, lines 40-41, Erhart et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shen et al.'s patent with the teachings of Erhart et al. by including an additional step of using the method wherein the computing step uses a linear feedback register to compute the syndromes. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method wherein the computing step uses a linear feedback register to compute the syndromes would provide the opportunity to use a programmable linear feedback register programmed with a feedback value corresponding to the generator polynomial and the programmable linear feedback register can be further programmed to receive the n bits of data and calculate syndromes.

12. Claims 8, 27, 28, 29, 33, 34, 35, 36, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) as applied to claim 1 and 25 above, and further in view of Stenerson (US 4,597,083).

As per claim 8, Shen et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Shen et al. do not explicitly teach the specific use of the method wherein the computing step includes the steps of: dividing a received code word in the data signal by a minimal Galois polynomial; and evaluating a remainder from said dividing step.

Stenerson in an analogous art teaches that codeword is divisible by a code generator polynomial in the form of a product of a plurality of different factors in the form (x+a.sup.i). Four syndrome signals are derived, each corresponding to a respective first order syndrome equal to the remainder upon dividing a received data block word by a respective factor (abstract, Stenerson).

Stenerson also teaches that the received codeword may be passed through a re-encoder (also known as a syndrome generator), which produces as its output the remainder of the polynomial division

s(x)=Remainder [R(x)/g(x)], (col. 4, lines 47-59, Stenerson).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shen et al.'s patent with the teachings of Stenerson by including an additional step of using the method wherein the computing step includes the steps of: dividing a received code word in the data signal by a minimal Galois polynomial; and evaluating a remainder from said dividing step.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method wherein the computing step includes the steps of: dividing a received code word in the data signal by a minimal Galois polynomial; and evaluating a remainder from said dividing step would provide the opportunity to determine error syndromes that can be used with further calculation to determine location of the errors and error values in the code word received.

- As per claim 27, Shen et al. and Stenerson teach the additional limitations.

Stenerson teaches the circuit wherein the using means computes a first correction term using at least one of the Galois field multiply accumulators, by assigning a value of a first one of the syndromes to the first correction term (col. 9, lines 44-46, col. 18, lines 28-33, Stenerson).

- As per claim 28, Shen et al. and Stenerson teach the additional limitations.

Stenerson teaches the circuit wherein the using means further computes a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes (col. 7, line 62-63, col. 18, lines 28-33, Stenerson).

- As per claim 29, Shen et al. and Stenerson teach the additional limitations.

Stenerson teaches the circuit wherein said using means computes the first correction term by operating at least one Galois field multiply accumulator in a pass-through mode (col. 18, lines 28-33, col. 22, lines 30-34, Stenerson).

- As per claim 33, Shen et al. and Stenerson teach the additional limitations.

Stenerson teaches the circuit wherein the using means uses the Galois field multiply accumulators to: compute a first correction term, by assigning a value of a first one of the syndromes to the first correction

term (col. 9, lines 44-46, col. 18, lines 28-33, Stenerson); and compute a second correction term, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes (col. 7, line 62-63, col. 18, lines 28-33, Stenerson).
Shen et al. teaches the circuit wherein the using means uses the Galois field multiply accumulators to compute a third correction term, the third correction term being based in part on coefficients of at least one of the minimum-degree polynomials (figure 4, col. 7, line 8 – col. 8, line 3, col. 12, lines 30-33, Shen et al.).

- As per claim 34, Shen et al. and Stenerson teach the additional limitations.

Shen et al. teach the circuit wherein the using means includes means for determining whether the second correction term is equal to zero (col. 7, lines 25-40, Shen et al.).

- As per claim 35, Shen et al. and Stenerson teach the additional limitations.

Shen et al. teach the circuit wherein said using means equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the second correction term is equal to zero (col. 7, line 7 – col. 8 line 3, Shen et al.).

- As per claim 36, Shen et al. and Stenerson teach the additional limitations.

Shen et al. teach the circuit wherein the using means includes means for determining whether the third correction term is equal to zero (col. 7, line 7 – col. 8 line 3, Shen et al.).

- As per claim 37, Shen et al. and Stenerson teach the additional limitations.

Shen et al. teach the circuit wherein the using means equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the third correction term is equal to zero. (col. 7, lines 8-15, Shen et al.).

13. Claims 15-17, 19, 20, 21, 22, 23, 40, 43, 44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) and Oh et al. (US 5,583,499) as applied to claim 13 and 38 above, and further in view of Stenerson (US 4,597,083).

As per claim 15, Shen et al. and Oh et al. substantially teach the claimed invention described in claim 13 (as rejected above).

However Shen et al. and Oh et al. do not explicitly teach the specific use of the method wherein the calculating step includes the step of computing a first correction term using at least one of the Galois field multiply accumulators, the first correction term being equal to a first one of the syndromes.
Stenerson in an analogous art teaches that assuming one error at location j, the error value e_j in relation to each syndrome is,
$S_{127} = e_j a^{127j}$ (col. 9, lines 44-46, Stenerson).
Stenerson also teaches that the Galois field products from multiplier 124 (in the form of a PROM programmed as shown in FIGS. 18C and 18D corresponding to multiplying by ff, the coefficient of the fourth term of the polynomial) are summed by exclusive-Ors 132 with the corresponding outputs of the latches 130 (col. 18, lines 28-33, Stenerson).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shen et al.'s patent with the teachings of Stenerson by including an additional step of using the method wherein the calculating step includes the step of computing a first correction term using at least one of the Galois field multiply accumulators, the first correction term being equal to a first one of the syndromes.
This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine the location of the error and the error value for the error location.

- As per claim 16, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Stenerson teach the method wherein said calculating step includes the step of computing a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes (col. 7, line 62-63, col. 18, lines 28-33, Stenerson).

- As per claim 17, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Stenerson teaches the method wherein the step of computing the first correction term includes the step of operating the at least one Galois field multiply accumulator in a pass-through mode (col. 18, lines 28-33, col. 22, lines 30-34, Stenerson).

- As per claim 19, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Stenerson teaches the method wherein said calculating step further includes the steps of: computing a first correction term using at least one of the Galois field multiply accumulators, the first correction term being equal to a first one of the syndromes (col. 9, lines 44-46, col. 18, lines 28-33, Stenerson); computing a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes (col. 7, line 62-63, col. 18, lines 28-33, Stenerson); and computing a third correction term using at least one of the Galois field multiply accumulators (col. 18, lines 35-43, Stenerson).

Shen et al. teach that the third correction term being based in part on coefficients of at least one of the minimum-degree polynomials (col. 7, line 8 – col. 8, line 3, Shen et al.).

- As per claim 20, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Shen et al. teach the method wherein said calculating step includes the step of determining whether the second correction term is equal to zero (col. 7, lines 25-40, Shen et al.).

- As per claim 21, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Shen et al. teach the method wherein the calculating step equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the second correction term is equal to zero (col. 7, line 7 – col. 8 line 3, Shen et al.).

- As per claim 22, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Shen et al. teach the method wherein the calculating step includes the step of determining whether the third correction term is equal to zero (col. 7, line 7 – col. 8 line 3, Shen et al.).

- As per claim 23, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Shen et al. teach the method wherein the calculating step equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the third correction term is equal to zero (col. 7, lines 8-15, Shen et al.).

- As per claim 40, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Stenerson teaches the decoder circuit wherein said state machine is programmed to operate a selected one or more of said Galois field multiply accumulators in a pass-through mode (col. 18, lines 28-33, col. 22, lines 30-34, Stenerson).

- As per claim 43, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Stenerson teaches the decoder circuit wherein equation (1) is performed using a first one of said Galois field multiply accumulators (col. 18, lines 28-35, Stenerson).

- As per claim 44, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Stenerson teaches the decoder circuit wherein equation (2) is performed using said first Galois field multiply accumulator and a second one of said Galois field multiply accumulators (col. 18, lines 28-35, Stenerson).

- As per claim 45, Shen et al., Oh et al. and Stenerson teach the additional limitations.

Stenerson teaches the decoder circuit wherein equation (3) is performed using said first and second Galois field multiply accumulators (col. 18, lines 28-35, Stenerson).

14. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) and Oh et al. (US 5,583,499) as applied to claim 38 above, and further in view of Wolf (US 6,385,751 B1).

As per claim 41, Shen et al. and Oh et al. substantially teach the claimed invention described in claim 38 (as rejected above).

However Shen et al. and Oh et al. do not explicitly teach the specific use of the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit.

Wolf in an analogous art teaches that Reed-Solomon encoders/decoders have been built using chip sets consisting of ASIC (Application Specific Integrated Circuit) processor elements (col. 3, lines 47-49, Wolf). Wolf also teaches that each of the blocks Reed-Solomon control block 403, Galois Field encoder setup block 422, Galois Field decoder setup block 423, encoder 457 and the decoder 458 illustrated in FIG. 4 include a state machine. The state machine flow is illustrated in FIG. 8 (figure 4, 8, col. 10, lines 50-54, Wolf).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shen et al.'s patent with the teachings of Wolf by including an additional step of using the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit would provide the opportunity to reduce the number of circuit elements and increase the processing speed of Galois field multiply accumulators and the decoder circuit for error correction.

15. Claims 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) and Oh et al. (US 5,583,499) as applied to claim 38 above, and further in view of Maki et al. (US 4,873,688).

As per claim 46, Shen et al. and Oh et al. substantially teach the claimed invention described in claim 38 (as rejected above).

However Shen et al. and Oh et al. do not explicitly teach the specific use of the decoder circuit wherein: at least one of said Galois field multiply accumulators has a first multiplexer whose output is coupled to a first input of a Galois field multiplier, a second multiplexer whose output is coupled to a second input of said Galois field multiplier, and a third multiplexer whose output is coupled to a first input of a Galois field adder, wherein an output of said Galois field multiplier is further coupled to a second input of said Galois field adder; and said state machine controls respective select lines for each of said multiplexers.

Maki et al. in an analogous art teach

"8. A Galois Field Euclid Algorithm apparatus for operating on an arbitrary received polynomial R(x), for calculating a magnitude polynomial, .OMEGA..sub.i (x) having a first plurality of coefficients and a location polynomial, .LAMBDA..sub.i (x), having a second plurality of coefficients, said magnitude polynomial representing a magnitude of an error in said received polynomial and said location polynomial

representing a location of said error in said received polynomial for use with a code having t correctable errors, said apparatus comprising:

a. a Euclid Algorithm divide module coupled to receive said received polynomial for implementing a first equation set forth below: .OMEGA..sub.i (x)=.OMEGA..sub.i-2 (x) mod .OMEGA..sub.i-1 (x); and

b. a Euclid Algorithm multiply module coupled to receive said received polynomial for implementing a second equation set forth below: .LAMBDA..sub.i (x)=-q.sub.i (x).LAMBDA..sub.i-1 (x)+.LAMBDA..sub.i-2 (x).

9. The Galois Field Euclid Algorithm apparatus according to claim 8 (Maki et al.) wherein:

a. said divide module comprises:

(1) a quotient bus;

(2) a plurality of first cells, each first cell having:

(a) a first input and a first output;

(b) a first register having a second input and a second output, said second input coupled to a said first input;

(c) a second register having a third input and a third output;

(d) a first 2 input/2 output multiplexer coupled to receive having a fourth input, a fifth input, a fourth output and a fifth output, said fourth input coupled to said second output, said fifth input coupled to said third output and said fourth output coupled said third input; and

(e) a first Galois Field multiplier having a sixth input, a seventh input and a sixth output, said sixth input coupled to said fourth output and to said third input and said seventh input coupled to said quotient bus;

(f) a Galois Field adder having an eighth input, a ninth input and a seventh output, said eighth input coupled to said sixth output, said ninth input coupled to said fifth output and said seventh output coupled to said first output; and

(3) a second cell having:

(a) a third register having a tenth input and an eighth output;

(b) a fourth register having an eleventh input and a ninth output;

(c) a second 2 input/2 output multiplexer having a twelfth input, a thirteenth input, a tenth output and an eleventh output said eighth output coupled to said twelfth input, said ninth output coupled to said thirteenth input and said eleventh output coupled to said eleventh input;

(d) means for calculating an inverse value having a twenty-second input and an eighteenth output, said twenty-second input coupled to said eighth output;

(e) a latch means having a twenty-third input and a nineteenth output, said twenty-third input coupled to said eighteenth output; and

(f) a second Galois Field multiplier having a twenty-fourth input, a twenty-fifth input and a twentieth output, said twenty-fourth input coupled to said nineteenth output, said twenty-fifth input coupled to said tenth output and said twentieth output coupled to said quotient bus; and

b. said multiply module comprises:

(1) said quotient bus; and

(2) a plurality of third cells, each said third cell having:

(a) a first register having a fourteenth input and a twelfth output;

(b) a second register having a fifteenth input and a thirteenth output;

(c) a third 2 input/2 output multiplexer having a sixteenth input, a seventeenth input, a fourteenth output and a fifteenth output, said sixteenth input coupled to said twelfth output;

(d) a Galois Field multiplier having an eighteenth input, a nineteenth input and a sixteenth output, said eighteenth input coupled to said fifteenth output and said nineteenth input coupled to said quotient bus; and

(e) a Galois Field adder having a twentieth input, a twenty-first input and a seventeenth output, said twentieth input coupled to said sixteenth output, said twenty-first input coupled to said fourteenth output and said seventeenth output coupled to said fourteenth input" (figure 9a, 9b, 9c, col. 19, line 12 – col. 20, line37, Maki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shen et al.'s patent with the teachings of Maki et al. by including an additional step of

using the decoder circuit wherein: at least one of said Galois field multiply accumulators has a first multiplexer whose output is coupled to a first input of a Galois field multiplier, a second multiplexer whose output is coupled to a second input of said Galois field multiplier, and a third multiplexer whose output is coupled to a first input of a Galois field adder, wherein an output of said Galois field multiplier is further coupled to a second input of said Galois field adder; and said state machine controls respective select lines for each of said multiplexers.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to use the Galois field multiply accumulators and multiplexers to generate an error polynomial that can be used to determine the location of errors in the code word.

- As per claim 47, Shen et al., Oh et al. and Maki et al. teach the additional limitations.

Maki et al. teach the decoder circuit further comprising means for determining when an output of said Galois field adder is equal to zero (col. 9, lines 22-30, Maki et al.)

16. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1) in view of Oh et al. (US 5,583,499).

As per claim 48, Alvarez et al. teach an 0C-192 input/output card comprising: four OC-48 processors; and an OC-192 front-end application-specific integrated circuit (ASIC) connected to said four OC-48 processors, said OC-192 front-end ASIC having means for de-interleaving an OC-192 signal to create four OC-48 signals (figure 17, page 12, paragraphs 192-193, page 30, paragraph 470, Alvarez et al.) However Alvarez et al. do not explicitly teach the specific use of means for decoding error-correction codes embedded in each of the four OC-48 signals, said decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles.

Oh et al. in an analogous art teach that for a t-error correcting Reed-Solomon coder 6t multipliers are needed in calculating the error locator polynomial using the Berlekamp-Massey algorithm, wherein t represents the error correcting capability of the code. The syndrome values are inputted every 2-symbol

clock cycles to be used in calculating the error locator polynomial. In other words, it takes two clock cycles in carrying out each iteration (col. 2, lines 19-25, Oh et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Oh et al. by including an additional step of using means for decoding error-correction codes embedded in each of the four OC-48 signals, said decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the time required to determine the locations of the errors.

17. Claims 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1) and Oh et al. (US 5,583,499) as applied to claim 48 above, and further in view of Stenerson (US 4,597,083).

As per claim 49, Alvarez et al. and Oh et al. substantially teach the claimed invention described in claim 48 (as rejected above).

However Alvarez et al. and Oh et al. do not explicitly teach the specific use of the decoding means that includes a plurality of Galois field multiply accumulators.

Stenerson in an analogous art teaches that the Galois field products from the multiplier 124 (in the form of a PROM programmed as shown in FIGS. 18C and 18D corresponding to multiplying by ff, the coefficient of the fourth term of the polynomial) are summed by exclusive-Ors 132 with the corresponding outputs of the latches 130 (figure 8, col. 18, lines 28-33, Stenerson).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Stenerson by including an additional step of using the decoding means that includes a plurality of Galois field multiply accumulators.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means that includes a plurality of Galois field multiply accumulators would provide the opportunity to generate an

error location polynomial and using the error location polynomial determine the location of errors in the code word.

- As per claim 50, Alvarez et al., Oh et al. and Stenerson teach the additional limitations.

Oh et al. teach that decoding means further includes a state machine for controlling (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

Stenerson teaches the Galois field multiply accumulators (figure 8, col. 18, lines 28-33, Stenerson).

18. Claims 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1), Oh et al. (US 5,583,499) and Stenerson (US 4,597,083) as applied to claim 49 above, and further in view of Shen et al. (US 6,199,188 B1).

As per claim 51, Alvarez et al., Oh et al. and Stenerson substantially teach the claimed invention described in claim 49 (as rejected above). Stenerson also teaches Galois field multiply accumulators (figure 8, col. 18, lines 28-33, Stenerson).

However Alvarez et al., Oh et al. and Stenerson do not explicitly teach the specific use of the decoding means to generate an error polynomial for a Bose-chaudhuri-Hbcquenghem (BCH) triple-error correcting code.

Shen et al. in an analogous art teach that there are essentially four major steps in decoding a corrupted code word of a Reed-Solomon code or a BCH code. The system first determines error syndromes that are based on the results of a manipulation of the ECC symbols. Next, using the error syndromes, the system determines an error locator polynomial, which is a polynomial that has the same degree as the number of errors (col. 1, lines 49-55, Shen et al.). Shen et al. also teach determining three error locations. In general, for any degree-three error locator polynomial, sigma(x), the system determines error locations (col. 7, lines 8-10, Shen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Shen et al. by including an additional step of using the decoding means to generate an error polynomial for a Bose-chaudhuri-Hbcquenghem (BCH) triple-error correcting code.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means to generate an error polynomial for a Bose-chaudhuri-Hbcquenghem (BCH) triple-error correcting code would provide the opportunity to determine error locations using the roots of the error polynomial.

- As per claim 52, Alvarez et al., Oh et al., Stenerson and Shen et al. teach the additional limitations.

Shen et al. teach that the decoding means includes no more than four of said Galois field multiply accumulators (col. 21, lines 19-21, col. 21, line 52 - col. 22, line 8, Shen et al.).

- As per claim 53, Alvarez et al., Oh et al., Stenerson and Shen et al. teach the additional limitations.

Stenerson teaches Galois field multiply accumulators (figure 8, col. 18, lines 28-33, Stenerson).
Shen et al. teach that decoding means includes means for computing a plurality of BCH syndromes which are used by said Galois field multiply accumulators to generate the error polynomial (figure 4, col. 1, lines 49-55, col. 12, lines 30-33, Shen et al.).

19. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1) and Oh et al. (US 5,583,499) as applied to claim 48 above, and further in view of Shen et al. (US 6,199,188 B1).

As per claim 54, Alvarez et al. and Oh et al. substantially teach the claimed invention described in claim 48 (as rejected above).

However Alvarez et al. and Oh et al. do not explicitly teach the specific use of the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers.

Shen et al. in an analogous art teach that in prior systems, the roots of degree-four polynomials are determined by trial and error, or by matrix manipulation or look-up table. The trial and error method is performed by substituting into the polynomial every possible value, i.e., every element of the applicable GF(2.sup.2m) that is associated with a code word location, and for each value evaluating the polynomial. If the polynomial equals zero for a given value, the value is a root. The system continues the trial and

error process by substituting a next possible value into the polynomial and determining if that value is a root; and so forth, until either all-possible values have been tried or all four roots are determined. This trial and error process, which in an optimized form is commonly known as a Chien Search, is time consuming. Further, the time is unpredictable, since it varies with the locations of the errors in the code words (col. 2, lines 1-15, Shen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Shen et al. by including an additional step of using the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers would provide the opportunity to determine the location of all the errors in the code word by determining all roots of the error locator polynomial.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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